MULTI-STAGE OUTPUT MULTIPLEXING CIRCUITS AND METHODS FOR DOUBLE DATA RATE SYNCHRONOUS MEMORY DEVICES

Abstract of the Disclosure

An output multiplexing circuit for a Double Data Rate (DDR) synchronous memory device includes n first latches, n first switches, n second switches, n second latches, and two third switches. The n first latches simultaneously prefetch n-bit data transmitted from a memory cell array via a data path. The n first switches simultaneously transfer the n-bit data prefetched into the first latches to n nodes in response to a CAS latency information signal. The n second switches simultaneously transfer data on the nodes in response to n signals that are synchronized with a clock signal and sequentially generated at a predetermined interval. The n second latches store the data transferred via the second switches. The two third switches sequentially transfer the data stored in the n second latches to an input terminal of an output driver of the memory device at a rising edge and a falling edge of a delay signal of the clock signal. Analogous methods also are described.